

FIG. 1B

System Processor

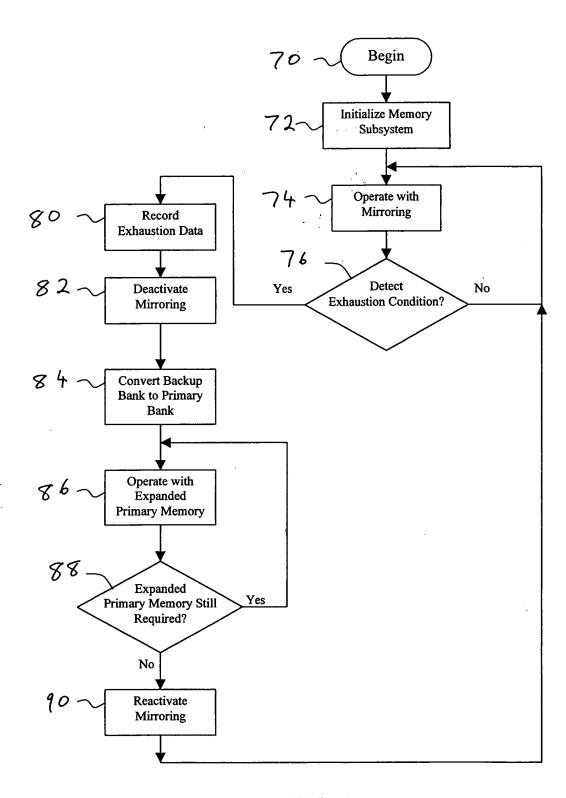
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| BSEL1 | BSEL0 | |
|-------|-------|--|
| 0 | . 0 | Mirror Bank0 on Bank3 |
| 0 | 1 | Mirror Bank1 on Bank3 |
| 1 | 0 | Mirror Bank2 on Bank3 |
| 1 | 1 | Use Bank3 as the high bank of a 4-bank array |

FIG. 3

| MR | |
|----|---|
| 0 | Read from primary bank |
| 1 | Read from Bank3 in lieu of primary bank |

FIG. 4



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FIG. 5